Amendments to the Specification

Please replace paragraph [0001] with the following amended paragraph:

[0001] This application is related to U.S. Patent Application Serial No. 09/977,089[[_____ (MIPS:0139.00US)]] entitled "CONFIGURABLE PRIORITIZATION OF CORE GENERATED INTERRUPTS", assigned to MIPS Technologies, Inc.

Please replace paragraph [0050] with the following amended paragraph:

[0050] The core 312 is responsible for executing instructions provided to the microprocessor 310 by a memory (not shown). In addition, the core 312 generates a number of core specific interrupts 314 (or internally generated interrupts), as will be further described below, to the vector generator 316. The vector generator 316 also receives the interrupts 306 provided by the interrupt controller 302 (e.g., externally generated interrupts). The vector generator 316 merges the prioritized interrupts 306 with the interrupts 314 generated by the core 312, and generates an interrupt vector 318 corresponding to the highest priority interrupt, as determined by the vector generator 316. A complete description of how the vector generator 316 prioritizes on-core and off-core interrupts, and generates an interrupt vector, is described in co-pending U.S. Patent Application Serial No. 09/977,089[[_____ (MIPS:0139.00US)]] entitled "CONFIGURABLE PRIORITIZATION OF CORE GENERATED INTERRUPTS" which is hereby incorporated by reference for all purposes.

Please replace paragraph [0064] with the following amended paragraph:

[0064] At this point it should be clear that the contents of GPR 1124 remain in the same state that they were in when the microprocessor 310 was interrupted. However, since the interrupt routine 1106 will use set "1" of the shadow set 1126, there is no need to save the contents of the GPR 1124 before the service routine 1106 is allowed to executed, because the service routine 1106 will not overwrite any of the contents of the GPR 1124. Rather, references by the service routine 1106 to registers within the GPR 1124 will utilize the duplicate registers within set "1" of the shadow set 1126.